Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. - 22. Cancelled.

23. – 30. Withdrawn.

31. – 46. Cancelled.

47. (Currently Amended) An optical logic circuit, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate the optical layer comprising a second material, the optical layer configured to provide a plurality of optical pathways, the optical pathways forming a plurality of optical logic gates, at least some of the optical logic gates having a first input that receives a constant coherent light input from a light source, a second input that receives a coherent light input which can be selectively turned on and off, an interference region coupled to the first and second light inputs, and an output coupled to the interference region opposite the first and second light inputs;

the interference region comprises the second material, the first and second optical inputs are spaced apart and the output is positioned such that an interference line is aligned with the output when the light input at the second input is on,

wherein the optical output signal is a Boolean logic output signal based on the second optical input signal and the optical output signal exits the interference region output.

48. (Previously Presented) The optical logic circuit of claim 47, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region through the output when the coherent light input to the second input is turned on.

49. (Previously Presented) The optical logic circuit of claim 47, wherein the interference region includes a third optical input receiving a coherent light input signal which can be selectively turned on and off.

50. (Previously Presented) The optical logic circuit of claim 49, wherein the interference region is configured to cause substantial cancellation of light exiting the output when coherent light is provided to the interference region through both the second optical input and the third optical input.

51. (Previously Presented) The optical logic circuit of claim 47, wherein the Boolean logic output is a NOT (inverter) function.

52. (Previously Presented) The optical logic circuit of claim 47, wherein the Boolean logic output is a NOT AND (NAND) function.

53. (Previously Presented) The optical logic circuit of claim 47, having a multiplicity of optical pathways and interference regions configured to function as an optical processor.

54. (Previously Presented) The optical logic circuit of claim 53, wherein the optical processor comprises NOT (inverter) gates and NOT AND (NAND) gates.

55. (Previously Presented) An optical logic gate for an optical processor, comprising:

a substrate configured of a first material;

a patterned optical layer overlaying the substrate, the optical layer comprising a second material, the patterned optical layer comprising a plurality of optical conduits formed of the second material, at least two of the optical conduits are configured to receive optical input signals, each of the optical input signals provide coherent light inputs, at least one of the optical conduits provides optical output signals, and at least one of the at least two optical input signals is a constant coherent light input signal; and

an interference region coupled to at least two of the optical conduits that are configured to receive optical input signals, the interference is caused along a predetermined axis

in the interference region, the interference region is coupled to at least one of the optical conduits configured to provide optical output signals, and the optical conduit receiving output signals is positioned such that the predetermined axis is aligned with the optical conduit receiving the output,

wherein the interference region is configured to provide a Boolean logic output signal based on one optical input signal that may selectively be turned on and off.

56. (Previously Presented) The optical logic gate of claim 55, wherein the optical logic gate provides a Boolean NOT function as output.

57. (Previously Presented) The optical logic gate of claim 55, further comprising:

at least three optical conduits configured to receive optical inputs.

58. (Previously Presented) The optical logic gate of claim 57, wherein the optical logic gate provides a Boolean NOT function as output.

59. (Previously Presented) The optical logic gate of claim 55, wherein the first material comprises silicon (Si).

60. (Previously Presented) The optical logic gate of claim 55, wherein the second material comprises doped silicon (Si).

61. (Previously Presented) The optical logic gate of claim 55, wherein the first material comprises Gallium Arsenide (GaAs).

62. (Previously Presented) The optical logic gate of claim 55, wherein the second material comprises doped Gallium Arsenide (GaAs).

63. (Previously Presented) The optical logic gate of claim 55, wherein the optical input signal is generated by a Laser diode.

64. (Previously Presented) The optical logic gate of claim 55, wherein the optical input signal is generated by a semiconductor diode.

65. (Currently Amended) A method of providing a Boolean logic optical output signal based on at least two optical input signals, comprising:

providing a first constant coherent light input signal to a first optical input such that the input signal is in an always on condition;

providing a plurality of optical pathways formed of optical transmission material patterned on a substrate material;

providing a second coherent light input signal, the second coherent light input signal being a coherent light input that is selectively turned on and off;

providing a distance between the plurality of optical pathways entering the interference region, the interference region enabling interference of the first constant coherent light input signal and the second coherent light input signal when the coherent light input signal is turned on; and

providing an optical output signal, the optical output signal is based on the ~~at least two~~ first constant coherent light input ~~signals~~ signal and the second coherent light input signal and is representative of a Boolean logic function.

66. (Previously Presented) The method of claim 65, wherein the Boolean logic function is a NOT (inverter) gate.

67. (Previously Presented) The method of claim 65, wherein the Boolean logic function is a NOT AND (NAND) gate.

68. (Previously Presented) The method of claim 65, wherein the Boolean logic function is configured of NOT (inverter) gates and NOT AND (NAND) gates.

69. (Currently Amended) An optical logic circuit, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate partially comprising a second material, the optical layer is patterned to provide a plurality of optical pathways, at least two optical pathways are configured to provide optical input signals, the optical input signals are coherent light inputs, and at least one optical pathway is configured to provide an optical output signal; and

an interference region configured to selectively cause interference of wavefronts of light from the optical input signals entering the interference region, the location of an interference line is based on the distance between the ~~first~~ at least two optical ~~pathway and the second optical pathway~~ pathways entering the interference region and the length of the interference region, the third optical pathway is positioned such that ~~the~~ an interference ~~line~~ line, caused by the interferences of wavefronts of light from the optical input signals entering the interference region, is aligned with the third optical pathway, the interference is produced along the interference line in the interference region,

wherein the interference region is configured to provide a Boolean logic output signal based on the at least two coherent light input signals.

70. (Previously Presented) The optical logic circuit of claim 69, wherein the interference region receives a first optical input that may be selectively turned on and off and a constant coherent light input.

71. (Previously Presented) The optical logic circuit of claim 69, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when a light signal is provided to the interference region through the coherent light input, the light signal being selected as on.

72. (Previously Presented) The optical logic circuit of claim 69, wherein the interference region includes a second coherent light input that may be selectively turned on and off.

73. (Currently Amended) The optical logic circuit of claim 69, wherein the interference region is configured to cause ~~substantial cancellation of~~ substantially no light exiting the interference region output when light is provided to the interference region through both the first ~~coherent~~ optical pathway ~~light input~~ and the second ~~coherent light input~~ optical pathway, and when no light is provided to both of the first and second ~~coherent light inputs~~ optical pathways.

74. (Previously Presented) The optical logic circuit of claim 69, wherein the Boolean logic output is a NOT (inverter) function.

75. (Previously Presented) The optical logic circuit of claim 69, wherein the Boolean logic output is a NOT AND (NAND) function.

76. (Previously Presented) The optical logic circuit of claim 69, having a multiplicity of optical pathways and interference regions configured to function as an optical processor.

77. (Currently Amended) The optical logic circuit of claim ~~69~~ 76 , wherein the optical processor is configured of NOT (inverter) gates and NOT AND (NAND) gates.

78. (Previously Presented) The optical logic circuit of claim 69, wherein the Boolean logic output is an XOR (exclusive OR) function.

Amendments to the Drawings:

The drawing sheet attached in connection with the above-identified application containing FIG. 9 is being presented as a new formal drawing sheet. The new drawing sheet (FIG. 9) was previously submitted in a fax RCE/Amendment of July 17, 2003, a copy of which is attached. Applicant requests entry of FIG. 9.